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**FACULTY DEVELOPMENT PROGRAMME (FDP)**  
**ON**  
**RECENT ADVANCEMENTS IN XILINX AND ASIC**  
**DESIGNS**

(16-12-2017 to 21-12-2017)

**Organized by**

**Department of ECE**

**JNTUA College of Engineering Anantapuramu (Autonomous)**  
**Anantapuramu, Sir Mokshagundam Vishweswarayya Road,**  
**Anantapuramu, Andhra Pradesh**

**in association with**

**National Institute of Technology, Warangal.**

**Under the Scheme of Electronics & ICT Academy**

**(Sponsored by Ministry of Electronics and Information Technology (MeitY), GOI)**



**Preamble:**

"Electronics & ICT Academy" was set up at NIT Warangal with financial assistance from MeitY, GoI. The jurisdiction of this academy is Telangana, Andhra Pradesh, Karnataka, Goa, Puducherry and Andaman & Nicobar Islands. This academy role is to offer faculty development programmes in standardized courses and emerging areas of Electronics, Information Communication Technologies, training & consultancy services for Industry, Curriculum development for Industry, CEP for working professionals, Advice and support for technical incubation and entrepreneurial activities.

**About the Workshop:**

As part of Electronics and ICT Academy initiative, a Faculty Development Programme (FDP) on Recent Advancements in Xilinx and ASIC Designs is being conducted to the faculty members of engineering colleges, industries and research laboratories

**Major Course Contents:**

- Describe the general Zynq / 7 Series All Programmable FPGA architecture
- Understand the Vivado design flow
- Create and debug HDL designs
- Configure FPGA and verify hardware operation
- Configure FPGA architecture features, such as Clock Manager, using the Architecture Wizard
- Use Logic Analyzer to perform on-chip verification
- ASIC Full custom & Semicustom IC Design flow using Mentor Graphics tools
- Design and Verification concepts using QuestaSim / Calibre Tools.

**Faculty conducting this programme:**

The programme will be conducted by the faculty members from NIT Warangal; Academicians in the concerned field from IITs/NITs/IIITs are invited to deliver lectures in the programme. Speakers from industries are also expected to deliver as part of the course.

**Eligibility:**

The programme is open to the teachers of Engineering Colleges, MCA Colleges and other allied disciplines in Telangana, Andhra Pradesh, Karnataka, Goa, Puducherry, Andaman and Nicobar Islands. Industry personnel working in the concerned /allied discipline can also attend.

**Registration Fee Particulars:**

Faculty and Research Scholars from Telangana, Andhra Pradesh, Karnataka, Puducherry, Andaman and Nicobar Islands, Goa	Rs. 2500/-
Faculty of SC/ST Category from Telangana, Andhra Pradesh, Karnataka, Puducherry, Andaman and Nicobar Islands, Goa	Rs. 1250/- (SC/ ST participants should submit the copy of their caste certificate to claim the concession along with application form)
Industry Participants	Rs. 7500/-
Participants from other states	Rs. 8500/-

SC/ST concession is only for faculty of mentioned states. Research Scholars are not eligible for SC/ST concession.

The participants need to send a crossed demand draft (DD) drawn in favor of "Director, NIT Warangal" and payable at SBH, NIT Warangal branch.

**Organized at:**

The programme will be coordinated and conducted by Department of Electronics and Communication Engineering of JNTUA College of Engineering, Anantapuramu, AP. The whole course is handled by academicians from premier institutions, Industry experts and Research advisors.

**Accommodation:**

All the selected participants will be provided FREE boarding & lodging in the institute guest house. No TA will be paid for the participants.

**How to apply:**

A filled-in form of application in the prescribed format duly signed and sponsored by appropriate authorities (along with demand draft) should reach the coordinator on or before the last date by post/courier. Participants are requested to write their name and contact number backside of demand draft. It is also mandatory to send scanned application form and demand draft through e-mail to vishnu.ece@jntua.ac.in and ravikumar@nitw.ac.in as selection will be intimated only through mail.

**Selection Criteria:**

Selection will be done based on first-come-first-serve basis to a maximum number of 50 (fifty). Additionally 10 participants from industry are allowed to participate. The list of selected participants will be intimated through e-mail. In case a candidate is not selected, the DD will be sent back. Candidates will be issued certificates on successful completion of the course. Reservations are followed for selecting candidates as per GOI norms.

**Important dates:**

Last date (Application & DD)	08 <sup>th</sup> December 2017
Selection List by E- mail	10 <sup>th</sup> December 2017
Duration of Program	16 <sup>th</sup> December to 21 <sup>st</sup> December 2017

**About NIT Warangal:**

National Institute of Technology, (formerly Regional Engineering College), Warangal is an Institute of National Importance and fully funded by MHRD, Govt. of India. It offers various programmes, B.Tech in eight branches, PG and M. Tech Programmes and also Ph.D. programmes.

**About JNTUA, Anantapuramu:**

JNTUA College of Engineering, established in the year 1946 is one of the prestigious institutions in India. The institute has a rich history and dedication to the pursuit of excellence. Over the years, there has been dynamic progress in all academic and research activities, and a parallel improvement in facilities and infrastructure, to keep it on par with the best institutions in the country. Though the College was initially established to provide basic technical education, with the passage of time, it emerged out, as one of the colleges to fulfil the technological need of our fast developing India with highly professional and well-trained graduates.

**About the Host department:**

The Electronics and Communication Engineering department is established in the year 1974. At present department is offering UG program in ECE and four full time PG programs in Digital Systems & Computer Electronics (DSCE), Digital Electronics & Communication Systems (DECS), VLSI System design and Embedded Systems specializations besides Ph.D. degree program in emerging areas of relevant technology.

**About CoreEL Technologies:**

CoreEL University Technologies is a CASPS technology company with business spread across design services & product development, distribution and training. Head Quartered in Bangalore, India, CoreEL is a leading provider of VLSI & Embedded Systems design services and Intellectual Property.



## APPLICATION FORM



### FACULTY DEVELOPMENT PROGRAMME(FDP) ON

RECENT ADVANCEMENTS IN XILINX AND

ASIC ODESIGNS

(16<sup>th</sup>– 21<sup>st</sup> December 2017)

Organized by

Department of ECE

JNTUA College of Engineering(Autonomous)

Anantapuramu

in association with

National Institute of Technology, Warangal.

1. Name :
2. Designation :
3. Institution :
4. Email :
5. DDNo: Bank: Date:

Amount:

6. Address forCorrespondence:

7. Educational Qualification:

8. Subjects taught sofar:

9. No. of refresher courses/workshopsattended:

10. Experience (inyears):

Teaching: Research: Industry:

11. Accommodation required: YES /NO

12. Do you belong to SC/ST : YES /NO

(If yes, please specify and attach a copy of caste certificate to claim the concession)

#### Declaration

The information provided is true to the best of my knowledge. If selected, I agree to abide by the rules and regulations of the FDP and shall attend the course for the entire duration. I also undertake the responsibility to inform the Coordinator in case, I am unable to attend the course.

Signature of the Applicant

#### SPONSORSHIP CERTIFICATE

Dr. /Mr. /Ms. .... is an employee of our Institute/Organization and is hereby sponsored to participate in the FDP on “**RECENT ADVANCEMENTS IN XILINX AND ASIC DESIGNS**”, sponsored by Electronics & ICT Academy during 16<sup>th</sup>Dec – 21<sup>st</sup> Dec 2017 at JNTUA College of Engineering(Autonomous) Ananthapuramu-515002.

Signature of Head of Institution  
(with seal)

#### Address for correspondence

Post your application form with DD to

**Dr. D. Vishnu Vardhan**  
Coordinator, FDP on RECENT ADVANCEMENTS IN XILINX  
AND ASIC DESIGNS

Department of Electronics & Communication Engineering  
JNTUA College of Engineering (Autonomous)  
Ananthapuramu, Andhra Pradesh State, India

E-mail the scanned copies of filled-in and duly signed  
application form along with DD to  
[vishnu.ece@jntua.ac.in](mailto:vishnu.ece@jntua.ac.in)

For more details about Electronics & ICT  
Academy, NIT, Warangal, please visit:  
<https://nitw.ac.in/eict>

For more enquiries please contact:  
Mobile: +91-9440221392

### Coordinators

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