JNTUA COLLEGE OF ENGINEERING (Autonomous), ANANTHAPURAMU
Department of Electronics & Communication Engineering
M. Tech (Regular) – VLSI SYSTEM DESIGN(VLSI SD)
(w. e. f 2016-17 Admitted Batch)

COURSE STRUCTURE

M. Tech I Semester

S.No	Sub. Code	Subject	Theory	Lab	Credits
1.	16D43101	Digital System Design	4	-	4
2.	16D43102	VLSI Technology and Design	4	-	4
3.	16D43103	CMOS Analog IC Design	4	-	4
4.	16D43104	CMOS Digital IC Design	4	-	4
5.	16D43105 15D41103 16D43106	**Elective-I** a) Analysis and Design of Digital Systems Through Verilog HDL b) Advanced Computer Architecture c) CAD for VLSI	4	-	4
6.	15D41206 16D43107 16D43108	**Elective-II** a) CPLD and FPGA Architectures and Applications b) Linux Programming & Scripting Languages c) Optimization Techniques in VLSI Design	4	-	4
7.	16D43109	VLSI System Design Lab	-	3	2
Contact periods/week			**24** Total/week	**03** **27**	**26**

M. Tech II Semester

S.No	Sub. Code	Subject	Theory	Lab	Credits
1.	15D41205	Low Power VLSI Design	4	-	4
2.	16D43201	CMOS Mixed Signal Design	4	-	4
3.	15D41201	Embedded System Design	4	-	4
4.	15D41211	Test and Testability	4	-	4
5.	16D43202 16D43203 16D43204	**Elective-III** a) System On chip Architectures b) Semiconductor Memory Design and Testing c) Design for Testability	4	-	4
6.	16D43205 16D43206 16D43207	**Elective-IV** a) System Verilog b) VLSI Signal Processing c) Physical Design Automation	4	-	4
7.	15D54201	Research Methodology (Audit Course)	2	-	-
8.	16D43108	System Verification Lab	-	3	2
Contact periods/week			**26** Total/Week	**03** **29**	**26**

M.Tech III & IV SEMESTERS

Code	Name of the Subject	C
	III Semester Seminar- I	2
	IV Semester Seminar- II	2
	III & IV Semester PROJECT WORK	44
	Total	**48**

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VLSI SYSTEM DESIGN

(16D43101) DIGITAL SYSTEM DESIGN

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

Learning Outcomes:
After completion of this course the students will be able to

- Complete knowledge regarding the minimization procedures employed in digital systems
- Apply minimization procedures for solving real world problems
- Build fault models for testing combinational and sequential circuits and Design fault models for testing digital systems
- Analyze different minimization procedures and fault models that are used with digital systems

UNIT-I
Minimization Procedures and CAMP Algorithm Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II
PLA Design, PLA Minimization and Folding Algorithms Introduction to PLDs, basic configurations and advantages of PLDs, PLA Introduction, Block diagram of PLA, size of PLA, LA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT–III
Design of Large Scale Digital Systems Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV
Fault Diagnosis in Combinational Circuits Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V

Fault Diagnosis in Sequential Circuits Fault detection and location in sequential circuits, circuit test approach, initial state identification, Hamming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXTBOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001,TMH
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS): ANANTHAPURAMU
VLSI SYSTEM DESIGN

(16D43102) VLSI TECHNOLOGY AND DESIGN

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

Course Outcomes:

After completion of the course the students will be able to

- Understand the fundamentals of CMOS VLSI design, and various electrical properties of MOS, BiCOMOS circuits
- Derive the expressions for various electrical properties of CMOS and BiCMOS circuits.
- Design small sub circuits using VLSI design technologies, FPGA, SoC.
- Analyze design concepts of combinational and sequential circuits

UNIT-I

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies, comparison of different processes.

UNIT-II

Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces. VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-III

Basic electrical properties of MOS and BiCMOS circuits: MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitatitive and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-IV

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations. Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.

UNIT-V

Floor Planning: Introduction, Floor planning methods, off-chip connections. Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing. Chip Design: Introduction and design methodologies.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, Sholeh Eshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, Phillip E.Allen, Noel R.Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin, CRC Press, 2011.
3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition, Addison Wesley
4. VLSI Design-Dr.K.V.K.K.Prasad, Kattula Shyamala, Kogent Learning Solutions Inc., 2012

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VLSI SYSTEM DESIGN

(16D43103) CMOS ANALOG IC DESIGN

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

Course Outcomes:

After completion of the course the students will be able to

- Understand significance of different biasing styles and apply them for designing analog ICs.
- Analyze the functionality of Current Mirrors, Current Sinks, Differential amplifiers and Current amplifiers.
- Design basic building blocks of analog ICs like, current mirrors, current sources, current sinks, two stage CMOS Power amplifiers and comparators.

UNIT –I

MOS Devices and Modeling: The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –III

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures, Mismatch-offset cancellation techniques, Reduction of Noise by offset cancellation techniques, Alternative definition of CMRR.

UNIT –IV

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT –V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce,
3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

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VLSI SYSTEM DESIGN

(16D43104) CMOS DIGITAL IC DESIGN

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

Course Outcomes:

After completion of the course the students will be able to

- Design CMOS inverters with specified noise margins and propagation
- Complete knowledge regarding the different issues associated with organization and design of semiconductor memories
- Realize and implement basic combinational and sequential elements that are commonly observed in digital ICs.
- Design basic combinational and sequential elements using NMOS and CMOS design strategies.
- Analyze the dynamic performance of CMOS circuits

UNIT-I

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits: Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

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ELECTIVE-I

(16D43105) ANALYSIS AND DESIGN OF DIGITAL SYSTEMS THROUGH VERILOG HDL

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

Course Outcomes:

After completion of the course the students will be able to

- Understand syntax of various commands available with verilog and fundamental associated with design of digital systems
- To design and simulate sequential and concurrent techniques in verilog and explain modeling of digital systems using verilog and design methodology
- Able develop problem solving skills and adapt them to solve real world problems
- Use computer as tool for solving research issues

UNIT-I

Digital Logic Design using Verilog HDL Introduction: Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

UNIT-II

Combinational Logic Circuit Design using Verilog: Combinational circuits building blocks: Multiplexers, Decoders , Encoders , Code converters, Arithmetic comparison circuits , Verilog for combinational circuits , Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look-Ahead Adder, Subtraction, Multiplication.

UNIT-III

Sequential Logic Circuit Design using Verilog: Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach.

UNIT-IV

Digital Logic Circuit Design Examples using Verilog: HDL Behavioral modeling , Data types, Boolean-Equation-Based behavioral models of combinational logics , Propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, Cyclic behavioral models

of flip-flops and latches and Edge detection, comparison of styles for b behavioral model; Behavioral model, Multiplexers, Encoders and Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations,

UNIT-V

ASM and ASMD charts for behavioral modeling: Design examples, Keypad scanner and encoder. Synthesis of Digital Logic Circuit Design Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.

TEXT BOOKS:

1. Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital logic design with Verilog", Tata McGraw Hill,2nd edition.

2. Michael D. Ciletti, "Advanced digital design with the Verilog HDL", Eastern economy edition, PHI.

REFERENCE BOOKS:

1. Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital logic with Verilog design", Tata McGraw Hill,2nd edition.
2. Bhaskar, "Verilog Primer",3rd Edition, PHI Publications.
3. Z.Navabi, VHDL Analysis and Modeling of Digital Systems, (2/e), McGraw Hill, 1998.
4. Douglos Perry, VHDL (3/e), McGraw Hill.2002

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ELECTIVE-I

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

(15D41103) ADVANCED COMPUTER ARCHITECTURE

Course objective:

- To study about various parallel computer models and also to study the program and network properties
- To study the concepts of pipelining and super scalar techniques.
- To study about architectures of multi processors and multi computers

Course ***Outcome:***

After completion of the course the students will be able to

- Know about different parallel computer models and their network properties.
- Understand about different concepts related to pipelining and super scalar techniques.
- Get complete knowledge regarding multi processors and multi computers.

UNIT - I

Parallel Computer Models – System attributes to performance, Multiprocessors and Multicomputers, Classifications of Architectures, Multivector and SIMD Computers, Architecture development tracks

UNIT - II

Program and Network Properties- Conditions for parallelism, Program partitioning and Scheduling, Program flow mechanisms, System interconnect architectures, Performance metrics and measures, Parallel Processing Applications

UNIT-III

Processors and Memory Hierarchy- Advanced Processor Technology, Superscalar and Vector processors, Memory hierarchy technology, Virtual Memory, Backplane bus systems, Cache memory organizations, Shared memory organizations

UNIT - IV

Pipelining and Superscalar Techniques Linear Pipeline processors, Nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design, Superscalar and Super Pipeline Design

UNIT- V

Multiprocessors and Multicomputers Multiprocessor System Interconnects, Cache Coherence and Synchronization mechanisms, Three generations of Multicomputers, Message passing mechanisms, Vector Processing principles, Principles of Multithreading

Text Books:

1. Hwang kai, "Advanced Computer Architecture", McGraw-Hill, 2001.
2. Patterson, David and Hennessy John, Morgn Kaufmann, "Computer Architecture",2001.

References:

1. William Stallings, Computer Organization and Architecture, 8th Edition, Prentice-Hall India, 2010.
2. David A Patterson and John L. Hennesey, Computer Organization and Design, 4th Edition, Elsevier India, 2011.
3. Andrew S Tanenbaum and James R Goodman, Structured Computer Organization, 5th Edition PrenticeHall India, 2009.

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ELECTIVE-I

(16D43106) CAD FOR VLSI DESIGN

M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

UNIT-I

VLSI Physical Design Automation VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II

Partitioning, Floor Planning, Pin Assignment and Placement Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing,

Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments,

UNIT-IV

Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Global Routing and Detailed Routing Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT-V

Physical Design Automation of FPGAs and MCMs FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.

2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.

2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.

3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

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VLSI SYSTEM DESIGN

ELECTIVE-II

(15D41206) CPLD AND FPGA ARCHITECURES AND APPLICATIONS

M.Tech II Sem	T	P	C
	4	0	4

UNIT-I
Introduction to Programmable Logic Devices Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II
Field Programmable Gate Arrays Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT–III
SRAM Programmable FPGAs Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT–IV
Anti-Fuse Programmed FPGAs Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT–V
Design Applications General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier,Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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ELECTIVE II

(16D43107) LINUX PROGRAMMING & SCRIPTING LANGUAGE

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

After completion of the course the students will be able to

- Understand basic commands of Linux that are required to work with linux.
- Understand basic commands of perl.
- Write scripts using perl for building CMOS desing

UNIT-I

Linux Basics: Introduction to Linux, File System of the Linux, General usage of Linux kernel 7 basic commands, Linux users and group, Permissions for file, directory and users, Searching a file & directory, Zipping and unzipping concepts.

UNIT-II

Overview of scripting language: PERL, File handles, Operators, Control structures, Regular expressions, Built in data types, Operators, Statements and declarations- simple, Compound, Loop statements, Global and scoped declarations.

UNIT-III

Pattern matching: Regular expression, Pattern matching operators, Character classes, Positions, capturing and clustering.

UNIT-IV

PERL built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT-V

Threads: Process model, Thread model, Perl debugger, Using debugger commands, Customization, Internals and externals, Internal data types, Extending perl, embedding perl, Exercises for programming using perl.

TEXT BOOKS:

1. Randal L, Schwartz Tom Phoenix, “Learning PERL”, Oreilly Publications, 3rd Edn., 2000

2. Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”, Oreilly ublications, 3rd Edn., 2000.

REFERENCE BOOKS:

1. Linux LRM.

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ELECTIVE II

(16D43108) OPTIMIZATION TECHNIQUES IN VLSI DESIGN

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

Course Outcomes:

After completion of the course the students will be able to

- Understand basics of statistical modeling
- Analyze performance of CMOS circuits with respect to power, area and speed
- Gets complete knowledge regarding the various algorithms used for optimization of power and area.

UNIT-I

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT-II

Statistical Performance, Power and Yield Analysis Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT-III

Convex Optimization Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting.

UNIT-IV

Genetic Algorithm Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm-unified algorithm.

UNIT-V

GA Routing Procedures and Power Estimation Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power -Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.

2. Genetic Algorithm for VLSI Design, Layout and Test Automation -Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.

REFERENCE BOOKS:

1. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004.

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(16D43109) VLSI SYSTEM DESIGN LAB

M.Tech I Sem	**T**	**P**	**C**
	0	**3**	**2**

Learning Outcomes:

After completion of this course the students will be able to

- Understand syntax of various commands available with verilog and fundamental associated with design of digital systems
- To design and simulate and implement various digital system like traffic light controller, UART.
- Able develop problem solving skills and adapt them to solve real world problems
- Write scripts using perl for building digital blocks

The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Single Port Synchronous RAM.
5. Synchronous FIFO.
6. ALU.
7. UART Model.
8. Dual Port Asynchronous RAM.

9. Fire Detection and Control System using Combinational Logic circuits.

10. Traffic Light Controller using Sequential Logic circuits

11. Pattern Detection using Moore Machine.

12. Finite State Machine (FSM) based logic circuit.

13. Perl Programming for basic operations.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Perl Software.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

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M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

(15D41205) LOW POWER VLSI DESIGN

After the completion of the course students will be able to

- Under stand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- Implement Low power design approaches for system level and circuit level measures.
- Design low power adders, multipliers and memories for efficient design of systems.

Fundamentals Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II

Low-Power Design Approaches Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III

Low-Voltage Low-Power Adders Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV

Low-Voltage Low-Power Multipliers Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V

Low-Voltage Low-Power Memories Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

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VLSI SYSTEM DESIGN

M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

(16D43201)CMOS MIXED SIGNAL DESIGN

After the Completion of the course the students will be able to

- Demonstrate first order filter with least interference
- Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- Design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT-I

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time- interleaved converters.

UNIT-V

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002

2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003

2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.

3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

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	4	**0**	**4**

(15D41201)EMBEDDED SYSTEM DESIGN

Course Outcome:
After completion of this course the students will be able to understand

- The issues relating to hardware and software design concepts associated with processor in Embedded Systems.
- The concept of low power microcontrollers.
- The hardware software co- design issues pertaining to design of an Embedded System using low power microcontrollers.

UNIT – I
Introductionto Embedded Electronic Systems and Microcontrollers:
An Embedded System-Definition, Embedded System Design and Development Life Cycle, An Introduction to Embedded system Architecture, The Embedded Systems Model, Embedded Hardware:The Embedded Board and the von Neumann Model, Embedded Processors: ISAArchitectureModels, Internal Processor Design, Processor Performance, Board Memory: Read-Only Memory (ROM), Random-Access Memory (RAM), Auxiliary Memory, Memory Management of External Memory and Performance, Approaches to Embedded Systems, Small Microcontrollers, Anatomy of a Typical Small Microcontroller, Small Microcontrollers Memory, Embedded Software, Introduction to small microcontroller (MSP430).

UNIT-II
MSP430 – I:
Architecture of the MSP430 Processor: Central Processing Unit, Addressing Modes, Constant Generator and Emulated Instructions, Instruction Set, Examples, Reflections on the CPU and Instruction Set, Resets, Clock System, Memory and Memory Organization.
Functions, Interrupts, and Low-Power Mode: Functions and Subroutines, Storage for Local Variables, Passing Parameters to a Subroutine and Returning a Result, Mixing C and Assembly Language, Interrupts, Interrupt Service Routines, Issues Associated with Interrupts, Low-Power Modes of Operation.

UNIT – III
MSP430 – II:
Digital Input, Output, and Displays: Parallel Ports, Digital Inputs, Switch Debounce, Digital Outputs, Interface between Systems, Driving Heavier Loads, Liquid Crystal Displays, Simple Applications of the LCD.
Timers: Watchdog Timer, Timer_A, Timer_A Modes, Timer_B,Timer_B Modes, Setting the Real-Time Clock, State Machines.

UNIT – IV

MSP430 Communication:

Communication Peripherals in the MSP430, Serial Peripheral Interface, SPI with the USI, SPI with the USCI, AThermometer Using SPI Modes,Inter-integrated Circuit Bus(I^2C) and its operations, State Machines for I^2C Communication, AThermometer Using I^2C, Asynchronous Serial Communication, Asynchronous Communication with the USCI_A, ASoftware UART Using Timer_A, Other Types of Communication.

UNIT – V

MSP430 Case Studies:

Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I^2C.

Text Books:

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005.
2. John H. Davies "MSP430 Microcontroller Basics",Elsevier Ltd Publications, Copyright 2008.

References:

1. Manuel Jiménez Rogelio,PalomeraIsidoroCouvertier "Introduction to Embedded SystemsUsing Microcontrollers and the MSP430" Springer Publications, 2014.
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.
3. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
4. Arnold S Burger, "Embedded System Design", CMP Books, 2002.
5. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications,Second Edition, 2008.

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M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

(15D41211)TESTING AND TESTABILITY

Course Outcome:
After completion of this course the students will be able to

- Understand different types of faults associated with logic circuits and types of testing by employing fault models to the logic circuits.
- Study about different methods of simulation and algorithms associated with testing.
- Get complete knowledge about different methods of simulation and algorithms associated with testing.

UNIT-I: Introduction to Testing
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II: Logic and Fault Simulation
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III: Testability Measures
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV: Built-In Self-Test
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V: Boundary Scan Standard
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

References:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Pulishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.
3. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

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M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

ELECTIVE-III

(16D43202) SOC ARCHITECTURES

Course Outcome:
After completion of this course the students will be able to

- Get complete basics related to SoC architecture and different approaches related to SoC Design.
- Able to select an appropriated robust processor for SoC Design
- Able to Select an appropriate memory for SoC Design.
- Design SoC
- Realize real time case studies

UNIT I:

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II:

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III:

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV:

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V:

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

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VLSI SYSTEM DESIGN

M.Tech II Sem	**T**	**P**	**C**
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ELECTIVE-III

(16D43203) SEMICONDUCTOR MEMORY DESIGN AND TESTING

After completion of the course the students will be able to

- Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.
- Able to build fault models for memory testing.
- Analyze different parameters that leads malfunctioning of memories.
- Design reliable memories with efficient architecture to improve processes times and power

UNIT-I

Random Access Memory Technologies SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II

Non-volatile Memories Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT-IV

Semiconductor Memory Reliability and Radiation Effects General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT-V

Advanced Memory Technologies and High-density Memory Packing Technologies Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.

REFERENCE BOOKS:

1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice all.

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M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

ELECTIVE-III

(16D43204)DESIGN FOR TESTABILITY

Course Outcome:
After completion of the course the student will be able to

- Get complete knowledge on different types of faults, fault models and different algorithms that can be employed for fault modeling.
- Built different fault models and analyze the using testability measures
- Design different types of built in self test pattern generators which aid for design of fault tolerant systems

UNIT-I
Introduction to Testing Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II
Logic and Fault Simulation Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT –III
Testability Measures SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV
Built-In Self-Test The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V
Boundary Scan Standard Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

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VLSI SYSTEM DESIGN

M.Tech II Sem	**T**	**P**	**C**
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ELECTIVE-IV

(16D43205)SYSTEM VERILOG

Course Outcome:
After completion of the course the student will be able to

- Get complete knowledge on principles of verification, and usage of System Verilog for verification
- Write test benches different layered architectures using system verilog
- Verify the functionality of different complex logics

UNIT 1
Verification Concepts: Importance of Verification, Concepts of Verification. Functional Verification process. Verification plan, Stimulus Generation. Test bench Generation, components and their performance, Coverage: Code and Functional coverage.

UNIT II
System Verilog – 1: Introduction to SV : Language evolution. Classes and objects. Class Variables and Methods. Class instantiation. Constructors. Inheritance. Derived classes. Data hiding and encapsulation. Polymorphism. System Verilog constructs - Data types: bit data, strings, arrays : queues, dynamic and associative arrays. New type creation. Structs, enumerated types. Routines for enumerated types. Statements. Procedural, continue and break statements. Tasks and functions. structures and unions, casting, Operators, Loops, Jumps, Program blocks. Processes and threads. IPC. Mailboxes and semaphore

UNIT III
System Verilog – 2: Modules, ports and interfaces. Communication with ports. Grouping signals. Clocking Blocks. Classes, Class Variables. Directed Vs Random Testing. Randomization. Constraint Driven Randomization. Coverage driven verification : Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

UNIT IV
Layered Test bench Architecture For Verification: Layered Test benches. Stimulus and Response.

Necessity for methodology. Verification Planning. Test bench architecture& Environment configuration : Generator, Driver, Receiver, Score board. assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Sequences and Assertion coverage

UNIT V

Verification of Architectural Building Blocks / Sub-Systems: Verification of Architectural building blocks and sub systems using system verilog: arbitration modules, arithmetic circuits, combinational and sequential blocks, data integrity, CDC, registers and memories.

REFERENCES:

1. Janick Bergeron, Writing Testbenches Using SystemVerilog

2. Chris Spear, SystemVerilog for Verification

3. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, Verification Methodology Manual for SystemVerilog

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VLSI SYSTEM DESIGN

M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

ELECTIVE-IV

(16D43206)VLSI SIGNAL PROCESSING

Course Outcomes:

After completion of the course the students will be able to

- Get indepth knowledge on signal processing system and various techniques of power reduction.
- Realize various adders, multipliers and filters and optimize their operation of by reducing the redundant operations
- Apply concept of pipelined architecture for various combinational and sequential circuit modules like adders, multipliers, filters
- Design Low Power IIR filters

UNIT-I

Transformations for retiming. Folding and unfolding DSP programs.

UNIT-II

Bit level arithmetic structures- parallel multipliers, interleaved floor plan and bit plan based digital filters. Bit serial multipliers. Bit serial filter design and implementation . Canonic signed digit arithmetic, Distributed arithmetic.

UNIT-III

Redundant arithmetic, redundant number representations , carry free radix 2 addition and subtraction . Hybrid radix 4 addition. Radix 2 hybrid redundant multiplication architectures , data format conversion. Redundant to nonredundant converter. Numerical strength reduction.

UNIT-IV

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems. Asynchronous pipelining.

UNIT-V

Scaling versus power consumption. Power analysis, power reduction techniques, power estimation techniques. Low power IIR filter design .Low power CMOS lattice IIR filter.

Text Book:

1. K.K. Parhi : VLSI Digital Signal Processing systems, John Wiley, 1999.

2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. 2. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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VLSI SYSTEM DESIGN

M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

ELECTIVE-IV

(16D43207) PHYSICAL DESIGN AUTOMATION

Course Outcomes:

After completion of the course the students will be able to

- Understand relation between automation algorithms and constraints posed by VLSI technology.
- Adopt algorithms to meet critical design parameters.
- Design area efficient logics by employing different routing algorithms and shape functions
- Simulate and synthesis different combinational and sequential logics

UNIT-I

VLSI design automation tools: algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.

UNIT-II

Layout compaction, placement and routing, Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.

UNIT-III

Floor planning and routing: floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

UNIT-IV

Simulation and logic synthesis: gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

UNIT-V

High-level synthesis: hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

Text Books:

1. S.H. Gerez, A lgorithms for VLSI Design Automation, John Wiley ,1998.
2. N.A.Sherwani , Algorithms for VLSI Physical Design Automation, (3/e), Kluwer,1999.

Reference Books:

1. S.M. Sait , H. Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

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M.Tech II Sem	**T**	**P**	**C**
	4	**0**	**4**

(15D54201) RESEARCH METHODOLOGY
(Audit Course)

UNIT I

Meaning of Research – Objectives of Research – Types of Research – Research Approaches – Guidelines for Selecting and Defining a Research Problem – research Design – Concepts related to Research Design – Basic Principles of Experimental Design.

UNIT II

Sampling Design – steps in Sampling Design –Characteristics of a Good Sample Design – Random Sampling Design.

Measurement and Scaling Techniques-Errors in Measurement – Tests of Sound Measurement – Scaling and Scale Construction Techniques – Time Series Analysis – Interpolation and Extrapolation.

Data Collection Methods – Primary Data – Secondary data – Questionnaire Survey and Interviews.

UNIT III

Correlation and Regression Analysis – Method of Least Squares – Regression vs Correlation – Correlation vs Determination – Types of Correlations and Their Applications

UNIT IV

Statistical Inference: Tests of Hypothesis – Parametric vs Non-parametric Tests – Hypothesis Testing Procedure – Sampling Theory – Sampling Distribution – Chi-square Test – Analysis of variance and Co-variance – Multi-variate Analysis.

UNIT V

Report Writing and Professional Ethics: Interpretation of Data – Report Writing – Layout of a Research Paper – Techniques of Interpretation- Making Scientific Presentations in Conferences and Seminars – Professional Ethics in Research.

Text books:

1. Research Methodology:Methods and Techniques – C.R.Kothari, 2nd Edition,New Age International Publishers.
2. Research Methodology: A Step by Step Guide for Beginners- Ranjit Kumar, Sage Publications (Available as pdf on internet)
3. Research Methodology and Statistical Tools – P.Narayana Reddy and G.V.R.K.Acharyulu, 1st Edition,Excel Books,New Delhi.

References:

1. Scientists must Write - Robert Barrass (Available as pdf on internet)
2. Crafting Your Research Future –Charles X. Ling and Quiang Yang (Available as pdf on internet)

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VLSI SYSTEM DESIGN

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	4	**0**	**4**

(16D43108) SYSTEM VERIFICATION LAB

PART-A: VLSI Lab (Back-end Environment)

The students are required to design and implement the Layout of the following experiments of any SIX using CMOS 130nm Technology.

List of Experiments:
1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static RAM Cell.
6. Dynamic RAM Cell.
7. ROM
8. Digital-to-Analog-Converter.
9. Analog-to-Digital Converter.

PART-B: Mixed Signal Simulation
The students are required to perform the following experimental concepts with suitable complexity mixed-signal application based circuits of any FOUR (circuits consisting of both analog and digital parts) using necessary software tools.

List of experimental Concepts:
• Analog circuit simulation.
• Digital circuit simulation.
• Mixed signal simulation.
• Layout Extraction.
• Parasitic values estimation from layout
• Layout Vs Schematic.
• Net List Extraction.
• Design Rule Checks.

Lab Requirements:
Software: Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool, Mixed Signal simulator

Hardware: Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

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Course Structure of R21 Academic Regulations for M.Tech (Regular) Programs with effect from AY 2021-2022

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI SYSTEM DESIGN

I SEMESTER

S.No.	Course Code	Subject Name	Cate Gory	Hours Per Week			Credits
				L	T	P	
1	21D43101	CMOS Analog IC Design	PC	3	0	0	3
2	21D42104	CMOS Digital IC Design	PC	3	0	0	3
3	**Professional Elective – I**						
	21D43102	Microchip Fabrication Techniques	PE	3	0	0	3
	21D42101	Advanced Digital System Design					
	21D43103	CAD for VLSI					
4	**Professional Elective – II**						
	21D43104	Device Modeling	PE	3	0	0	3
	21D43105	FPGA Architecture and Applications					
	21D43106	ASIC Design					
5	21D11109	Research Methodology and IPR	MC	2	0	0	2
6	21D11110	English for Research Paper Writing	AC	2	0	0	0
	21D11111	Value Education					
	21D11112	Pedagogy Studies					
7	21D43107	CMOS Analog IC Design Lab	PC	0	0	4	2
8	21D43108	CMOS Digital IC Design Lab	PC	0	0	4	2
Total				**16**	**00**	**08**	**18**

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI SYSTEM DESIGN

II SEMESTER

S.No.	Course Code	Subject Name	Cate Gory	Hours Per Week			Credits
				L	T	P	
1	21D43201	CMOS Mixed Signal IC Design	PC	3	0	0	3
2	21D43202	Physical Design Automation	PC	3	0	0	3
3	**Professional Elective – III**						
	21D42204	SoC Architecture	PE	3	0	0	3
	21D43203	Semiconductor Memory Design and Testing					
	21D42203	Low Power VLSI Design					
4	**Professional Elective – IV**						
	21D43204	Bi-CMOS Technology and Applications	PE	3	0	0	3
	21D43205	System Verilog					
	21D43206	VLSI Signal Processing					
5	21D11209	Technical Seminar	PR	0	0	4	2
6	21D11210	Disaster Management	AC	2	0	0	0
	21D11211	Constitution of India					
	21D11212	Stress Management by Yoga					
7	21D43207	CMOS Mixed Signal IC Design Lab	PC	0	0	4	2
8	21D43208	Physical Design Automation Lab	PC	0	0	4	2
Total				**14**	**00**	**12**	**18**

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI SYSTEM DESIGN

III SEMESTER

S.No.	Course Code	Subject Name	Cate Gory	Hours Per Week			Credits
				L	T	P	
1	**Professional Elective – V**						
	21D43301	RFIC Design	PE	3	0	0	3
	21D43302	Optimization Techniques and Applications in VLSI Design					
	21D43303	SoC Testing and Verification					
2	**Open Elective**						
	21D40301	Network Security and Cryptography	OE	3	0	0	3
3	21D43304	Dissertation Phase – I	PR	0	0	20	10
4	21D00301	Co-Curricular Activities	PR				2
Total				**06**	**00**	**20**	**18**

IV SEMESTER

S.No.	Course Code	Subject Name	Cate Gory	Hours Per Week			Credits
				L	T	P	
1	21D43401	Dissertation Phase – II	PR	0	0	32	16
Total				**00**	**00**	**32**	**16**

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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D43101	CMOS ANALOG IC DESIGN (21D43101)	L	T	P	C
Semester	I		3	0	0	3

Course Objectives:

- This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
- Basic design concepts, issues and trade-offs involved in analog IC design are explored.
- Intuitive understanding and real-life applications are emphasized throughout the course.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.
- To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

Course Outcomes (CO): Student will be able to

- Design MOSFET based analog integrated circuits.
- Analyzeanalog circuits at least to the first order.
- Appreciate the trade-offs involved in analog integrated circuit design.
- Understand and appreciate the importance of noise and distortion in analog circuits.
- Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area

UNIT - I Lecture Hrs:

Significance of analog IC Design, challenges under deep submicron environment.
Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Layout and stick diagrams.
Basic building blocks - Sources, Sinks and References.

UNIT - II Lecture Hrs:

Single Stage Amplifiers: Basic Concepts, Common Source Stage, Source Degeneration, Single stage Common Source amplifier with diode connected load and current source load, Source follower, Common Gate Stage, Biasing styles, Limitations of single stage amplifiers, Gain boosting techniques: Design of Cascodeamplifier, Regulated Cascode topology.

UNIT – III Lecture Hrs:

Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads. Passive and Active Current Mirrors – Basic Current Mirrors, Inaccuracies of Current mirror, Replication principle,Cascode Current Mirrors, Active Current Mirrors.

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UNIT – IV		Lecture Hrs:
Frequency Response of Amplifiers: General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.		
UNIT – V		Lecture Hrs:
Feedback Amplifiers and Op-amp: General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – Characterization of Op-amp, Two Stage Op-amps, Dominant pole compensation, Pole splitting, Effect of right-hand plane zero, Fully compensated op-amp against process and temperature variations.Common – Mode Feedback.		
Textbooks:		
1. 1. B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill Edition, 2nd Edition. 2. T.C. Carusone, D.A. Johns and K. Martin, "Analog Integrated Circuit Design", Wiley, 2nd Edition.		
Reference Books:		
1. Paul.R. Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition. 2. P.E. Allen&D.R. Holberg, "CMOS Analog Circuit Design",Oxford University Press, 3rd Edition. 3. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Wiley, 3rd Edition. 4. Adel S. Sedra, Kenneth C. Smith, Arun, "Microelectronic Circuits",Oxford University Press, 6th Edition.		
Online Learning Resources:		

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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D42104	CMOS DIGITAL IC DESIGN (21D42104)	L	T	P	C
Semester	I		3	0	0	3

Course Objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Course Outcomes (CO): Student will be able to

- Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,
- Estimate Delay and Power of Adders circuits.
- Classify different semiconductor memories.
- Analyze, design and implement combinational and sequential MOS logic circuits.
- Analyze complex engineering problems critically in the domain of digital IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area of digital ICs

UNIT - I		Lecture Hrs:

CMOS Inverter and Pseudo NMOS Logic characterization: Characterization of CMOS Inverter, Noise Margin, Inverter threshold voltage, Transient response, Pseudo NMOS logic gates, Transistor equivalence, Design of CMOS Inverter driving large capacitive loads.

UNIT - II		Lecture Hrs:

Combinational MOS Logic Circuits:MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT - III		Lecture Hrs:

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT - IV		Lecture Hrs:

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT - V		Lecture Hrs:

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

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(VLSI SYSTEM DESIGN)

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, PHI,2nd Edition.

Online Learning Resources:

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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D43102	MICROCHIP FABRICATION TECHNIQUES (21D43102)	L	T	P	C
Semester	I		3	0	0	3

Course Objectives:

- Comprehend impact of semiconductor industry on the design of development of integrated circuits.
- Acquaint with clean room technology
- Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
- Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and 45nm technologies
- Understand packaging principles

Course Outcomes (CO): Student will be able to

- Understand various stages of fabrication
- Understand various packaging techniques and Design rules.
- Classify various thin films and its characteristics.

UNIT - I		Lecture Hrs:

Introduction to Processing: Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, clean room construction.

UNIT - II		Lecture Hrs:

Photolithography: Oxidation and Photolithography, ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT - III		Lecture Hrs:

Diffusion & Ion Implantation: Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT - IV		Lecture Hrs:

Film Depositions and Growth: Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT - V		Lecture Hrs:

Yield: Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.
Packaging: Chip characteristics, package functions, package operations.

Textbooks:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 6th Edition.
2. S.M. Sze, VLSI technology, McGraw-Hill Book Company, 2nd Edition.

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(VLSI SYSTEM DESIGN)

Reference Books:
1. Wani-Kai Chen (editor), The VLSI Handbook, CRI/IEEE press, 2000. 2. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2nd Edition.
Online Learning Resources:

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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D43105	FPGA ARCHITECTURES AND APPLICATIONS (21D43105) PE – I	L	T	P	C
Semester	I		3	0	0	3

Course Objectives:

- To acquire knowledge about various architectures and device technologies of PLD's.
- To comprehend FPGA Architectures.
- To analyze System level Design and their application for Combinational and Sequential Circuits.
- To familiarize with Anti-Fuse Programmed FPGAs.
- To apply knowledge of this subject for various design applications.

Course Outcomes (CO): Student will be able to

- Acquire knowledge about various architectures and device technologies of PLD's.
- Comprehend FPGA Architectures.
- Analyze System level Design and their application for Combinational and Sequential Circuits.
- Familiarize with Anti-Fuse Programmed FPGAs.
- Apply knowledge of this subject for various design applications.

UNIT - I		Lecture Hrs:

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT - II	**Field Programmable Gate Arrays**	Lecture Hrs:

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT - III		Lecture Hrs:

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT - IV		Lecture Hrs:

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT - V		Lecture Hrs:

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Textbooks:

1. Stephen M. Trimberger,"Field Programmable Gate Array Technology", Springer International Edition.
2. Charles H. Roth Jr, LizyKurianJohn,"Digital Systems Design", Cengage Learning, 3rd Edition.

Reference Books:

1. John V. Oldfield, Richard C. Dorf,"Field Programmable Gate Arrays", Wiley India.
2. Pak K. Chan, SamihaMourad, "Digital Design Using Field Programmable Gate Arrays", Pearson Low Price Edition.
3. Ian Grout,"Digital Systems Design with FPGAs and CPLDs", Elsevier, Newnes.
4. Wayne Wolf,"FPGA based System Design", Prentice Hall Modern Semiconductor Design Series.

Online Learning Resources:

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D43107	CMOS ANALOG IC DESIGN LAB	L	T	P	C
Semester	I	(21D43107)	0	0	4	2

Course Objectives:

- To explain the VLSI Design Methodologies using VLSI design tool.
- To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
- To explain the Physical Verification in Layout Design
- To fully appreciate the design and analyze of analog and mixed signal simulation
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

Course Outcomes (CO):

- Explain the VLSI Design Methodologies using VLSI design tool.
- Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
- Explain the Physical Verification in Layout Design
- Fully appreciate the design and analyze of analog and mixed signal simulation
- Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

LIST OF EXPERIMENTS:

- The students are required to design and implement the following Experiments using CMOS 130nm Technology.
- The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.
    1. Familiarization of tool and design flow with the help of simple CMOS inverter design
    2. MOS Device Characteristics (evaluation of channel length modulation coefficient λ) and parametric analysis
    3. Common Source Amplifier with current source load and diode connected load
    4. Common Source Amplifier with source degeneration
    5. Cascode amplifier
    6. Simple current mirror
    7. Cascode current mirror.
    8. Differential Amplifier with current source load
    9. Differential Amplifier with current mirror load
    10. Design of nine transistor Amplifier (Dominant pole compensation)

Lab Requirements:

Software: Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator, Cadence tools

Hardware: Personal Computer with necessary peripherals, configuration and operating System.

References:

Online learning resources/Virtual labs:

Course Code	21D43108	CMOS DIGITAL IC DESIGN LAB	L	T	P	C

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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Semester	I	(21D43108)	0	0	4	2

Course Objectives:

- To explain the VLSI Design Methodologies using any VLSI design tool.
- To grasp the significance of various design logic Circuits in full-custom IC Design.
- To explain the Physical Verification in Layout Extraction.
- To fully appreciate the design and analyze of CMOS Digital Circuits.
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Course Outcomes (CO):

- Explain the VLSI Design Methodologies using any VLSI design tool.
- Grasp the significance of various design logic Circuits in full-custom IC Design.
- Explain the Physical Verification in Layout Extraction.
- Fully appreciate the design and analyze of CMOS Digital Circuits.
- Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

LIST OF EXPERIMENTS:

The students are required to design and implement the following experiments at the Circuit level and synthesize the same using appropriate FPGA.

1. CMOS InverterCharacteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software: Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware: Personal Computer with necessary peripherals, configuration and operating System.

References:

Online learning resources/Virtual labs:

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(VLSI SYSTEM DESIGN)

Course Code	21D43201	CMOS MIXED SIGNAL IC DESIGN (21D43201)	L	T	P	C
Semester	II		3	0	0	3

Course Objectives:

- To demonstrate first order filter with least interference
- To extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- To design different A/D, D/A, modulators, demodulators and different filter for real time applications

Course Outcomes (CO): Student will be able to

- Demonstrate first order filter with least interference
- Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- Design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT - I Lecture Hrs:

Significance of Mixed signal design and challenges in scale down technologies.
Review of basic building blocks, fully compensated op-amps, Principle of bandgap reference.
Comparators: Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

UNIT-II Lecture Hrs:

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT – III Lecture Hrs:

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT - IV Lecture Hrs:

Data Converter: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT - V Lecture Hrs:

A to D Converters: Characterization of ADC, Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters.
Oversampling Converters: Noise shaping modulators, Decimating filters and

interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A.
Textbooks:
1. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2nd Edition. 2. Philip E. Allen and Douglas R. Holberg,"CMOS Analog Circuit Design", Oxford University Press, International Second Edition/Indian Edition, 2010. 3. David A. Johns, Ken Martin,"Analog Integrated Circuit Design", Wiley Student Edition, 2013.
Reference Books:
1. Rudy Van De Plassche, "CMOS Integrated Analog-to- Digital and Digital-to-Analog converters", Kluwer Academic Publishers, 2nd Edition. 2. Richard Schreier, "Understanding Delta-Sigma Data converters", Wiley, 2nd Edition. 3. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", Wiley, 2nd Edition.
Online Learning Resources:

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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D43202	PHYSICAL DESIGN AUTOMATION (21D43202)	L	T	P	C
Semester	II		3	0	0	3

Course Objectives:

- To understand relation between automation algorithms and constraints posed by VLSI technology.
- To adopt algorithms to meet critical design parameters.
- To design area efficient logics by employing different routing algorithms and shape functions.
- To simulate and synthesis different combinational and sequential logics.

Course Outcomes (CO): Student will be able to

- Understand relation between automation algorithms and constraints posed by VLSI technology.
- Adopt algorithms to meet critical design parameters.
- Design area efficient logics by employing different routing algorithms and shape functions.
- Simulate and synthesis different combinational and sequential logics.

UNIT - I Lecture Hrs:

VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT - II Lecture Hrs:

Layout: Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT - III Lecture Hrs:

Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT - IV Lecture Hrs:

Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, two level logic synthesis.

UNIT - V Lecture Hrs:

High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

Textbooks:

1. S.H. Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1998.
2. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer, 3rd Edition.

Reference Books:

1. S.M. Sait,H. Youssef, “VLSI Physical Design Automation”, World scientific, 1999.

2. M. Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996.
Online Learning Resources:

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D42204	SOC ARCHITECTURE (21D42204)	L	T	P	C
Semester	II	PE – III	3	0	0	3

Course Objectives:

- To understand the basics related to SoC architecture and different approaches related to SoC Design.
- To select an appropriate robust processor for SoC Design
- To select an appropriate memory for SoC Design.
- To realize real time case studies

Course Outcomes (CO): Student will be able to

- Understand the basics related to SoC architecture and different approaches related to SoC Design.
- Select an appropriated robust processor for SoC Design
- Select an appropriate memory for SoC Design.
- Realize real time case studies

UNIT - I | Lecture Hrs:

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT - II | Lecture Hrs:

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT - III | Lecture Hrs:

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV | Lecture Hrs:

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT - V | Lecture Hrs:

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

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Textbooks:

1. "Computer System Design System-on-Chip", Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. "ARM System on Chip Architecture", Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

Reference Books:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer.
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

Online Learning Resources:

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R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D43205	SYSTEM VERILOG (21D43205)	L	T	P	C
Semester	II	PE – IV	3	0	0	3

Course Objectives:

- To understand the principles of verification, and usage of System Verilog for verification
- To write test benches different layered architectures using system Verilog
- To verify the functionality of different complex logics

Course Outcomes (CO): Student will be able to

- Get complete knowledge on principles of verification, and usage of System Verilog for verification
- Write test benches different layered architectures using system Verilog
- Verify the functionality of different complex logics

UNIT - I Lecture Hrs:

Verification Concepts: Importance of Verification, Concepts of Verification. Functional Verificationprocess. Verification plan, Stimulus Generation. Test bench Generation, components and theirperformance, Coverage: Code and Functional coverage

UNIT - II Lecture Hrs:

System Verilog – 1: Introduction to SV: Language evolution. Classes and objects. Class Variables andMethods. Class instantiation. Constructors. Inheritance. Derived classes. Data hiding andencapsulation. Polymorphism. System Verilog constructs - Data types: bit data, strings, arrays:queues, dynamic and associative arrays. New type creation. Structs, enumerated types. Routines forenumerated types. Statements. Procedural, continue and break statements. Tasks and functions.structures and unions, casting, Operators, Loops, Jumps, Program blocks. Processes and threads. IPC.Mailboxes and semaphore

UNIT - III Lecture Hrs:

System Verilog – 2: Modules, ports and interfaces. Communication with ports. Grouping signals.
Clocking Blocks. Classes, Class Variables. Directed Vs Random Testing. Randomization. ConstraintDriven Randomization. Coverage driven verification: Motivation, Types of coverage, Cover Group,Cover Point, Cross Coverage, Concepts of Binning and event sampling.

UNIT - IV Lecture Hrs:

Layered Test bench Architecture for Verification: Layered Test benches. Stimulus and Response. Necessity for methodology. Verification Planning. Test bench architecture&Environmentconfiguration: Generator, Driver, Receiver, Score board. assertions: Introduction to Assertion basedverification, Immediate and concurrent assertions. Sequences and Assertion coverage

UNIT - V Lecture Hrs:

Verification of Architectural Building Blocks / Sub-Systems: Verification of Architectural building blocks and sub systems using system Verilog: arbitration modules, arithmetic circuits, combinational and sequential blocks, data integrity, CDC, registers and memories

R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Textbooks:
1. Janick Bergeron, Writing Testbenches Using SystemVerilog, Springer. 2. Chris Spear, "SystemVerilog for Verification: A Guide to Learning the Testbench Language Features", Springer, 2nd Edition.
Reference Books:
1. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, "Verification, Methodology Manual for SystemVerilog", Springer.
Online Learning Resources:

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS) :: ANANTHAPURAMU
Ananthapuramu – 515 002, Andhra Pradesh, India

R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D43207	CMOS MIXED SIGNAL IC DESIGN LAB (21D43207)	L	T	P	C
Semester	II		0	0	4	2

Course Objectives:

- To design and simulate op-amp for given specifications
- To design and simulate data converter for given specifications
- To design and simulate PLL and VCO for given specifications
- To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Course Outcomes (CO):

- Design and simulate op-amp for given specifications
- Design and simulate data converter for given specifications
- Design and simulate PLL and VCO for given specifications
- Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

LIST OF EXPERIMENTS:

The students are required to design and implement the Circuit and Layout of thefollowing Experiments using CMOS 130nm Technology.

Cycle 1:

1. Fully compensated op-amp with resistor and miller compensation
2. High speed comparator design
    a. Two stage cross coupled clamped comparator
    b. Strobed Flip-flop
3. Data converter

Cycle 2:

1. Switched capacitor circuits
    a. Parasitic sensitive integrator
    b. Parasitic insensitive integrator
2. Design of PLL
3. Design of VCO
4. Band gap reference circuit
5. Layouts of All the circuits Designed and Simulated

Software: Mentor Graphics/Cadence/Tanner/Industry Equivalent Standard Software Tools

Hardware: Personal Computer with necessary peripherals, configuration and operating System.

References:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley,1986.
3. Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

Online learning resources/Virtual labs:

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS) :: ANANTHAPURAMU
Ananthapuramu – 515 002, Andhra Pradesh, India

R21 COURSE STRUCTURE &SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(VLSI SYSTEM DESIGN)

Course Code	21D43208	PHYSICAL DESIGN AUTOMATION LAB (21D43208)	L	T	P	C
Semester	II		0	0	4	2

Course Objectives:

- To learn the implementation of different Physical Design Automation algorithms
- To implement different graph algorithms
- To implement different partitioning algorithms
- To implement different floor planning algorithms
- To implement different routing algorithms

Course Outcomes (CO):

- Learn the implementation of different Physical Design Automation algorithms
- Implement different graph algorithms
- Implement different partitioning algorithms
- Implement different floor planning algorithms
- Implement different routing algorithms

LIST OF EXPERIMENTS:

Cycle 1:

1. Graph algorithms
    a) Graph search algorithms
        i. Depth first search
        ii. Breadth first search
    b) Spanning tree algorithm
        i. Kruskal‟s algorithm
    c) shortest path algorithm
        i. Dijkstra algorithm
        ii. Floyd- Warshall algorithm
    d) Steiner tree algorithm
2. Computational geometry algorithm
    a) Line sweep method
    b) Extended line sweep method

Cycle 2:

3. Partitioning algorithms
    a) Group migration algorithms
        I. Kernighan –Lin algorithm
        II. Extensions of Kernighan-Lin algorithm
            i) Fiduccias –Mattheyses algorithm
            ii) Goldberg and Burstein algorithm
    b) Simulated annealing and evolution algorithms

i. Simulated annealing algorithm
ii. Simulated evolution algorithm
III) Metric allocation method

4. Floor planning algorithms
   i) Constraint based methods
   ii) Integer programming-based methods
   iii) Rectangular dualization based methods
   iv) Hierarchical tree-based methods
   v) Simulated evolution algorithms
   vi) Time driven Floor planning algorithms

5. Routing algorithms
   I) Two terminal algorithms
      a) Maze routing algorithms
         i)Lee‟s algorithm
         ii) Soukup‟s algorithm
         iii) Hadlock algorithm
      b) Line-Probe algorithm
      c) Shortest path based algorithm
   II) Multi terminal algorithm
      a) Steniertree based algorithm
         i) SMST algorithm
         ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Textbooks:

1. NaveedShervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2. Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.

References:

Online learning resources/Virtual labs:

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS) :: ANANTHAPURAMU
Ananthapuramu – 515 002, Andhra Pradesh, India

R21 COURSE STRUCTURE & SYLLABUS FOR M.TECH COURSES
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS)

Course Code	21D42302	IoT AND ITS APPLICATIONS (PE – V)	L	T	P	C
Semester	III		3	0	0	3

Course Objectives:

1. To apply the Knowledge in IOT Technologies and Data management.
2. To determine the values chains Perspective of M2M to IOT.
3. To educate building blocks and characteristics of Internet of Things
4. To introduce communication protocols used in Internet of Things
5. To impart knowledge on design & develop IoT devices

Course Outcomes (CO): Student will be able to

1. Apply the Knowledge in IOT Technologies and Data management.
2. Determine the values chains Perspective of M2M to IOT.
3. Examine communication protocols used in IoT
4. Make use of python programming to implement Internet of Things
5. Design IoT applications using Raspberry Pi

UNIT - I **Lecture Hrs:**

Introduction to IoT: Introduction, Physical Design of IoT, Logical Design of IoT, IoT Enabling Technologies.
Domain Specific IoTs: Home Automation, cities, Environment, Energy, Retail, Logistics, Agriculture, Industry, Health & Lifestyle

UNIT - II **Lecture Hrs:**

Fundamentals of IoT:
IoT Network Architecture and Design: Drivers Behind New Network Architectures, Comparing IoT Architectures, Simplified IoT Architecture, Core IoT Functional Stack, IoT Data Management and Compute Stack
Smart Objects: Sensors, Actuators, and Smart Objects, Sensor Networks.

UNIT - III **Lecture Hrs:**

IoT Communication Protocols:
Communications Criteria: Range, Frequency Bands, Power Consumption, Topology, Constrained Devices, Constrained-Node Networks, Data Rate and Throughput, Latency and Determinism, Overhead and Payload.
IoT Access Technologies: IEEE 802.15.4, IEEE 1901.2a, IEEE 802.11ah, LoRaWAN, NB-IoT and other LTE Variations

UNIT - IV **Lecture Hrs:**

IoT Network Layer Protocols: Need for Optimization – Constrained Nodes, Constrained Networks, IP versions Optimizing IP for IoT - From 6LoWPAN to 6Lo, Header Compression, Fragmentation, Mesh addressing
IoT Application Layer Protocols: CoAP, MQTT

UNIT - V **Lecture Hrs:**

IOT Physical Devices & Endpoints: What is an IOT Device, Exemplary Device, About the Board, Linux on Raspberry Pi, Raspberry Pi Interfaces, Programming Raspberry Pi with Python; Python web application framework – Django, Designing a Restful web API.

Textbooks:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities Press,2015

Reference Books:

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence", Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.

Online Learning Resources: